UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,145	04/14/2004	Daniel James Winarski	TUC920040007US1	7857

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EXAMINER
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ART UNIT	PAPER NUMBER
2186	

NOTIFICATION DATE	DELIVERY MODE
06/06/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)
Office Action Summary	10/825,145	WINARSKI ET AL.
	Examiner	Art Unit	
	MICHAEL C. KROFCHECK	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _17 April 2008_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,4-13,15 and 18_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,4-13,15 and 18_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _14 April 2008_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to the RCE filed on 4/17/2008.

2.   Claims 1, 5-6, and 15 have been amended.

3.   The objections/rejections from the prior correspondence not restated herein have

been withdrawn.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
        obviousness or nonobviousness.

6.   This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

7.   Claims 1, 5-8, 10, 12-13 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Kopsaftis (5659801), Torrey et al. (2003/0084240), and Goodman et

al. (20040054883).

8.   With respect to claims 1 and 6, Kopsaftis teaches of a method for updating

microcode in an automated data storage library, comprising the steps of: assigning a

first logical unit number (LUN) to a first device, wherein the first device is an input/output

device of said automated data storage library (fig. 1; column 5, lines 29-37; where the

commands directed to the disk drive, 10 are received by the bus interface as they

contain the same LUN as stored in the bus interface. Thus the disk drive device must

have been assigned a LUN);

said first device receiving a plurality of commands (fig. 1; column 5, lines 29-37;

where the commands directed to the disk drive, 10 are received by the bus interface as

they contain the same LUN as stored in the bus interface);

wherein said first LUN processes I/O commands (column 4, lines 1-16);

said first device obtaining a LUN address from each of said plurality of

commands (fig. 1; column 5, lines 29-37; where the commands directed to the disk

drive, 10 are received by the bus interface as they contain the same LUN as stored in

the bus interface);

in response to said LUN address obtained from each of said plurality of commands being equal to said first LUN, processing each of said plurality of commands as input/output commands of said first device (fig. 1; column 5, lines 29-37, 47-62); and

in response to said first device receiving a prepare for microcode update command, placing said first device in an operational state to receive said update of said microcode (column 8, lines 63-65).

Kopsaftis fails to explicitly teach of assigning a second LUN to a memory. However, Torrey teaches of assigning a first LUN to a first I/O device; assigning a second LUN to a memory, wherein said memory is memory of said I/O device (fig. 2; paragraph 15-16; where the library is LUN 1-0 or LUN 0 and the drives may be LUNs 1-1, 1-2, or LUNs 1, 2);

wherein said first LUN and said second LUN are separate (fig. 2; paragraph 15-16; as the library has a LUN and the drives have different LUNs they are individually distinguishable and thus separate);

said first device obtaining a LUN address from each of said plurality of commands (fig. 3; paragraph 19-20)

The combination of Kopsaftis and Torrey teaches of said second LUN processes microcode update commands (Kopsaftis, fig. 1, 3; column 8, line 63-column 9, line 2; in the combination the internal memories are assigned LUNs, and are thus accessed via them Torrey, paragraph 16, 19-20);

in response to said LUN address obtained from each of said plurality of commands being equal to said second LUN, storing said microcode in said memory

using said LUN address assigned to said memory by processing each of said plurality of commands, thereby updating said stored microcode in said first device (Kopsaftis, fig. 1, 3; column 5, lines 29-37, column 8, line 63-column 9, line 15; Since in the combination, each command contains the LUN of where it is applied (Torrey paragraph 19-20) the initiator command and subsequent microcode upgrade commands would contain the LUN for the appropriate memory).

Kopsaftis fails to explicitly teach of directly overwriting said microcode in said memory.

However, Goodman teaches of directly overwriting said microcode in said memory (fig. 4; paragraph 14-15, 46).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis and Torrey at the time of the invention to assign the different types of storage in Kopsaftis different LUNs as taught in Torrey. Their motivation would have been to facilitate control of multiple devices and assist in upgrades Torrey (paragraphs 4-5).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis, Torrey, and Goodman at the time of the invention to directly overwrite the prior microcode of the combination of Kopsaftis and Torrey as taught in Goodman. Their motivation would have been to more efficiently use and access the memory.

9.   With respect to claim 5, Kopsaftis teaches of wherein said processing each of said plurality of commands to update said microcode further comprises: overwriting said

memory associated with said first device with an updated microcode (fig. 3, item 236; column 10, lines 25-37).

10.   With respect to claim 7, Kopsaftis teaches of a host, wherein said host sends microcode update commands to said first device (fig. 1; item 20; column 1, lines 25-29, column 3, lines 32-43).

11.   With respect to claim 8, Kopsaftis teaches of a host (fig. 1; item 20; column 3, lines 32-43); and

        a device interface coupled to said host wherein said device interface receives commands from said host and transfers said commands to LUN addressable components (fig. 1; item 40; column 3, lines 32-43; column 3, line 66-column 4, line 3; as the commands are sent to the disk drive (LUN addressable components) from the host, it must be done through the SCSI interface as it is the only connection between the two).

12.   With respect to claim 10, Kopsaftis teaches of wherein said memory is coupled to said first device (fig. 1, items 108, 10; where the memory 108 is connected to the bus interface and all the other components of the disk drive, thus being coupled to the disk drive (first device)).

13.   With respect to claim 12, Kopsaftis teaches of a second device removably attached to said first device, wherein said memory is coupled to said second device (fig. 1; item 60; where the SCSI bus, 60, is attached to the disk drive. It is abundantly clear to one of ordinary skill in the art that the bus is removably attached to the disk drive, as disk drives the cables connecting them to the bus can be disconnected from the each

other in a computer. As such the non-volatile memory, 108 is attached to it through the bus interface).

14.   With respect to claim 13, Kopsaftis teaches of a controller for operating said first device, wherein said memory is coupled to said controller (fig. 1; items 106, 112).

15.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, and Goodman as applied to claim 1 above, and further in view of Shirasawa et al. (2002/0166027).

16.   With respect to claim 4, Kopsaftis fails to explicitly teach of not accepting any new commands for processing; completing all current commands; and placing movable components at a rest position. However, Shirasawa teaches of wherein said placing said first device in an operational state to receive said update of said microcode further comprises: not accepting any new commands for processing; completing all current commands (fig. 3, paragraph 0038-0039; where the I/O process to the hard disk A is stopped. It is abundantly clear to one of ordinary skill in the art that the command currently being executed are finished as if they were abruptly stopped, that can result in corrupting the data on the drive); and

placing movable components at a rest position (fig. 3, paragraph 0038-0039; It is abundantly clear to one of ordinary skill in the art that as all access to the drive has stopped and that a reboot of the drive will be necessary upon completion of the firmware update, initially powering down the spindle motor, arm, etc. would conserve considerable power while the firmware is being updated).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis, Torrey, Goodman, and Shirasawa at the time of the invention to enable the transferring of I/O processing to another drive when updating the firmware of a specific drive in the combination of Kopsaftis, Torrey, and Goodman as taught in Shirasawa. This would enable current I/O processing to continue uninterrupted (Shirasawa, paragraph 0012).

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, and Goodman as applied to claim 6 above, and further in view of Pellegrino et al. (2004/0225775).

18. With respect to claim 9, Kopsaftis fails to explicitly teach of said memory is an EEPROM. However, Pellegrino teaches of wherein said memory is an Electrically Erasable Programmable Read Only Memory (paragraph 0030).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis, Torrey, Goodman, and Pellegrino at the time of the invention to make the non-volatile memory of the combination of Kopsaftis, Torrey, and Goodman an EEPROM as taught in Pellegrino as numerous devices have embedded their firmware in EEPROM so that it can be updated, and will not be lost when power is removed from the memory (Pellegrino, paragraph 0030).

19. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, and Goodman as applied to claim 6 above, and further in view of Abbott et al. (6205093).

20.   With respect to claim 11, Kopsaftis fails to explicitly teach of an accessor. However, Abbott teaches of further comprising an accessor, wherein said memory is coupled to said accessor (fig. 2; item 18; column 4, lines 18-35).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis, Torrey, Goodman, and Abbott at the time of the invention to store and update the microcode of Abbott in a non-volatile memory as taught in the combination of Kopsaftis, Torrey and Goodman, implementing the microcode updating method in a tape system as Kopsaftis teaches of the system also using tapes, column 1, lines 6-24. This would simplify the processing of sending separate management and data I/O commands over the same interface in the tape system and provide increased speed by using a solid state memory over a disk drive to store the microcode in.

21.   Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Kopsaftis, Torrey, Goodman, and Burton et al. (6393535).

22.   With respect to claim 15, the combination of Kopsaftis, Torrey, and Goodman teaches of all the limitations cited above with respect to claims 1 and 6. Burton teaches of an article of manufacture comprising a data storage medium tangibly embodying a program of machine-readable instruction executed by a processing apparatus to perform method steps (column 9, lines 35-53).

It would have been obvious to one of ordinary skill in the art having the teachings of Kopsaftis, Torrey, Goodman, and Burton at the time of the invention to implement the method steps from the combination of Kopsaftis and Torrey, and Goodman in the

information bearing media of Burton. Their motivation would have been to allow for the

process to be easily transferred and implemented on different computer systems.

23.   Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Kopsaftis, Torrey, Goodman, and Burton as applied to claim 15 above, and further in

view of Shirasawa.

24.   With respect to claim 18, Shirasawa teaches of the limitations cited above with

respect to claim 4.

        It would have been obvious to one of ordinary skill in the art having the teachings

of Kopsaftis, Torrey, Goodman, Burton, and Shirasawa at the time of the invention to

enable the transferring of I/O processing to another drive when updating the firmware of

a specific drive in the combination of Kopsaftis, Torrey, Goodman, and Burton as taught

in Shirasawa. This would enable current I/O processing to continue uninterrupted

(Shirasawa, paragraph 0012).

Response to Arguments

25.   Applicant's arguments filed 4/17/2008 have been fully considered but they are

not persuasive.

26.   In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., "in response to said first device receiving a prepare for microcode update

command, placing said first device in an operational state to receive said update of said

microcode") are not recited in the rejected claim (claim 6).   Although the claims are

interpreted in light of the specification, limitations from the specification are not read into

the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

27.   Applicant argues with respect to the independent claims (claims 1, 6, and 15)

that the combination of Kopsaftis, Torrey, Goodman, and Burton (in claim 18), does not

teach of (1) in response to the LUN address obtained from each of the plurality of

commands being equal to the second LUN, directly overwriting the microcode in the

memory using the LUN address assigned to the memory by processing each of the

plurality of commands, thereby updating the stored microcode in the first device, and (2)

in response to the first device receiving a prepare for microcode update command,

placing the first device in an operational state to receive the update of the microcode.

The examiner disagrees with this.

In response to (1), Torrey in paragraph 19-20 teaches that each command

indicates the LUN of the memory that it is to be applied to. Applying this to the initiator

and microcode upgrade commands of Kopsaftis (disclosed in column 5, lines 29-37,

column 8, line 63-column 9, line 15) the initiator and microcode upgrade commands

would contain the required LUN, and cause the microcode upgrade to occur. The

combination in view of Goodman, directly overwriting the old microcode in the memory

with the new microcode (Goodman, fig. 4; paragraph 14-15, 46).

In response to (2), Kopsaftis explicitly teaches this in column 8, lines 63-65

stating, "when the initiator command is detected...the disk drive enters a state ready to

receive new microcode." Fig. 4 of Kopsaftis shows the initiator command detector

connected to the bus interface (first device) that detects the initiator command.

28.   Applicant argues with respect to claims 4 and 18 that the combination of Kopsaftis, Torrey, Goodman, Burton (in claim 18), and Shirasawa does not teach of placing a first device in an operational state to receive the update of the microcode which further comprises not accepting any new commands for processing; completing all current commands; and placing movable components at a rest position.

The examiner disagrees. Paragraphs 38-39 of Shirasawa teaches of halting all I/O processes to the hard disk prior to updating the hard disk's firmware. It is abundantly clear to one of ordinary skill in the art to finish currently executing I/O processes because if they were abruptly stopped, the data on the drive may become corrupt. It is also obvious to one of ordinary skill in the art that since there are no longer I/O processes occurring in the hard drive, that the heads and arms of the hard drive are not moving since they are not reading, writing, or searching for data.

Conclusion

29.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

30.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL C KROFCHECK/   /Matt Kim/
Examiner, Art Unit 2186   Supervisory Patent Examiner, Art
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